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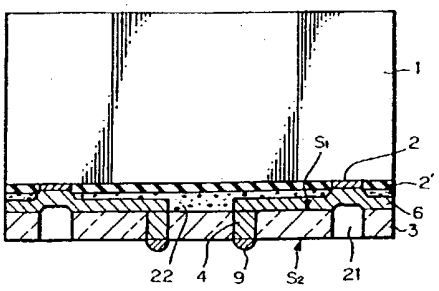
(54) Method for manufacturing bump leaded film carrier type semiconductor device.

(57) An insulating film (3) has conductive layers (6) on a first surface (S_1) and conductive protrusions (9) on a second surface (S_2). The conductive layers (6) are connected to the conductive protrusions (9) via through holes provided in the insulating film. A semiconductor chip (1) having pads (2) is adhered by an adhesive layer (22) to the insulating film (3). Then, the conductive layers (6) are locally pressured, so that the conductive layers (6) are electrically connected to respective ones of the pads (2).

Fig. 5A



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(54) **Method for manufacturing bump leaded film carrier type semiconductor device**

Herstellungsverfahren einer mit Anschlusshöckern versehenen Halbleiteranordnung vom Filmträgertyp

Procédé de fabrication d'un dispositif semi-conducteur du type à bande de support avec plots de connexion

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method for manufacturing a bump leaded film carrier type semiconductor device.

Description of the Related Art

[0002] New semiconductor packages have been developed to correspond to requirements of electronic apparatuses which are of a smaller size, of a smaller weight, of a higher speed and of a higher function. In order to satisfy such requirements, it is necessary to reduce the pitch of inner leads, i.e., portions of leads connected to a semiconductor chip, simultaneously with the adoption of an area array bonding system capable of enlarging the pitch of outer leads.

[0003] One typical inner lead bonding (ILB) system is a wire bonding system which, however, cannot correspond to the increased number of multi-pins and the narrowed pitch of pads of the semiconductor chip. Recently, a tape automated bonding (TAB) system has been broadly used to reduce the size of semiconductor devices. In the TAB system, inner leads made of metal foil by etching an insulating film are bonded to conductive protrusions (bumps) formed on pads of a chip.

[0004] One typical area array bonding system is a flip-chip bonding system. In the flip-chip bonding system, solder bumps are formed on an active element surface of a chip, and then, the chip is reversed and is bonded directly to a substrate, thus corresponding to multi-pins and small-pitched pins. In this case, the length of bonded connections is so short that there is an advantage in high speed and low noise.

[0005] In the above-described bonding systems, a process for forming barrier metal and bumps on electrode pads of a bare chip is generally required. For example, when solder is applied as bump material for aluminum electrodes, Cr or Ti as an adhesive layer and Cu, Ni, Rh or Pd as a diffusion avoiding layer have to be formed on electrode faces by a sputtering method or an evaporation method. Also, a step for forming bumps made of solder or Au by ball bumps or by plating is required. Further, in the TAB system, a transfer bump system or mesa bump system for bonding bumps formed on inner leads has been suggested.

[0006] In order to make use of both of the advantages of the TAB system and the flip-chip bonding system, first prior art bump leaded film carrier type semiconductor devices have been suggested where bumps are formed on a chip facing side of an insulating film (see: JP-A-SHO53-56969, JP-A-HEI5-47847, JP-A-HEI2-229445). This will be explained later in detail.

[0007] In the first prior art bump leaded film carrier type semiconductor devices, however, outer leads, i.e., portions of leads connected to a substrate extend to the outside, and as a result, there is a disadvantage in size.

[0008] Second prior art bump leaded film carrier type semiconductor devices have also been suggested where bumps are formed on a substrate facing side of an insulating film (see: JP-A-HEI4-154136, JP-A-HEI5-82586). In the second prior art bump leaded film carrier semiconductor devices, since outer leads extend toward the inside, the second prior art bump leaded film carrier type semiconductor devices can be reduced in size as compared with the first prior art bump leaded film carrier type semiconductor devices. This will be explained later in detail.

[0009] In the second prior art bump leaded film carrier type semiconductor devices, however, the deformation of the insulating film is very large, or the devices are still large in size.

[0010] In PATENT ABSTRACTS OF JAPAN, vol. 17, no. 687 (E-1478), 16. December 1993; & JP-A-5-235091, a method for realising a flip chip is described wherein inner lead bonding leads formed on a film carrier tape and connected to electrode bumps and an outer lead bonding bump mount where the flip chip is mounted are provided.

[0011] In PATENT ABSTRACTS OF JAPAN, vol. 17, no. 415 (E-1407), 3. August 1993; & JP-A-5-082586, a semiconductor device is described wherein bump electrodes of a semiconductor chip are joined to contact points of an insulating board and wherein the chip and a surface of the board are sealed cup with a sealing resin package main body.

[0012] The WO 92/11654 describes a leadless pad array chip carrier package which has a protective plastic cover transfer molded about a semiconductor device.

[0013] In R. Tummula, E. Rymaszewski "Microelectronics Packaging handbook", van Nostrand Reinhold, New Yord, 1989, 419-423, two primary options of a bump structure are described.

SUMMARY OF THE INVENTION

[0014] It is an object of the present invention to provide a method for manufacturing a bump leaded film carrier type semiconductor device which can be firm as well as small in size.

[0015] This object is solved by the methods of claims 1, 7, or 8. Thus, the device can be made firm by the combination of the semiconductor chip and the insulating film using the adhesive layer. Simultaneously, since the adhesive layer can be thin, the device can be small in size. Further advantageous embodiments and improvements are mentioned in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present invention will be more clearly understood from the description as set forth below, as com-

pared with the prior art, with reference to the accompanying drawings, wherein:

Fig. 1 is a cross-sectional view illustrating a first prior art bump leaded film carrier type semiconductor device;

Figs. 2A and 2B are cross-sectional views illustrating a modification of the device of Fig. 1;

Fig. 3 is a cross-sectional view illustrating a second prior art bump leaded film carrier type semiconductor device;

Fig. 4 is a cross-sectional view illustrating a modification of the device of Fig. 3;

Fig. 5A is a cross-sectional view illustrating a first embodiment of the bump leaded film carriertype semiconductor device according to the present invention;

Fig. 5B is a bottom view of the device of Fig. 5A;

Fig. 6A is a plan view of a film carrier for explaining the manufacturing steps of the device of Fig. 5A;

Fig. 6B is a bottom view of the film carrier of Fig. 6A;

Figs. 7A through 7H are cross-sectional views for explaining the manufacturing steps of the device of Fig. 5A;

Fig. 8 is a partially-enlarged cross-sectional view of the device of Fig. 7C;

Fig. 9A is a cross-sectional view illustrating a second embodiment of the bump leaded film carrier type semiconductor device according to the present invention;

Fig. 9B is a bottom view of the device of Fig. 9A;

Fig. 10A is a plan view of a film carrier for explaining the manufacturing steps of the device of Fig. 9A;

Fig. 10B is a bottom view of the film carrier of Fig. 9A;

Figs. 11A through 11H are cross-sectional views for explaining the manufacturing steps of the device of Fig. 9A;

Fig. 12 is a partially-enlarged cross-sectional view of the device of Fig. 11C;

Fig. 13A is a cross-sectional view illustrating a third embodiment of the bump leaded film carrier type semiconductor device according to the present invention;

Fig. 143 is a bottom view of the device of Fig. 13A;

Fig. 14A is a cross-sectional view illustrating a fourth embodiment of the bump leaded film carrier type semiconductor device according to the present invention;

Fig. 14B is a bottom view of the device of Fig. 14A;

Fig. 15A is a plan view of the insulating film of Figs. 13A, 13B and 14A, 14B;

Fig. 15B is a bottom view of the insulating film of Figs. 13A, 13B and 14A, 14B;

Fig. 16A is a cross-sectional view illustrating a fifth embodiment of the bump leaded film carrier type semiconductor device according to the present invention;

Fig. 16B is a bottom view of the device of Fig. 16A;

Figs. 17A through 17G are cross-sectional views for explaining the manufacturing steps of the device of Fig. 16A;

Fig. 18 is a cross-sectional view illustrating a sixth embodiment of the bump leaded film carriertype semiconductor device according to the present invention;

Figs. 19A and 19B are cross-sectional views illustrating a seventh embodiment of the bump leaded film carrier type semiconductor device according to the present invention; and

Fig. 19C is a bottom view of the device of Figs. 19A and 19B.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Before the description of the preferred embodiments, prior art bump leaded film carrier type semiconductor devices will be explained with reference to Figs. 1, 2A, 2B, 3 and 4.

[0018] In Fig. 1, which illustrates a first prior art bump leaded film carrier type semiconductor device (see: JP-A-SHO53-56969, JP-A-HEI5-47847), reference numeral 1 designates a bare chip having pads 2. Also, reference numeral 3 designates an insulating film made of polyimide or the like. Throughholes are perforated by a photolithography and etching process or a pressing process in the insulating film 3, and conductive members 4 are fitted into the through holes. Also, conductive

protrusions, i.e., bumps 5 coupled to the conductive members 4 are provided on a first surface S1 of the insulating film 3. On the other hand, conductive layers 6 coupled to the conductive members 4 are provided on a second surface S2 of the insulating film 3.

[0019] In the device of Fig. 1, however, outer leads (not shown) of the conductive layers 6 are located outside of the chip 1, which increases the device of Fig. 1 in size. Also, since the support of the chip 1 to the insulating film 3 is carried out by only the bonding of the pads 2 to the bumps 5, the mechanical strength of the device is deteriorated.

[0020] In Figs. 2A and 2B, which illustrate a modification of the device of Fig. 1 (see: JP-A-HEI2-229445), means for improving contact characteristics of the chip 1 to the insulating film 3 is added to the elements of the device of Fig. 1. That is, a thermal adhesive resin layer 7 is formed on a pad forming face of the chip 1, while openings 8 are provided in the insulating film 3. When the chip 1 is bonded to the insulating film 3, the contact characteristics of the chip 1 to the insulating film 3 is improved, and simultaneously, the chip 1 can be electrically protected.

[0021] In the device of Figs. 2A and 2B, however, since the outer leads (not shown) are still located outside of the chip 1, the device of Figs. 2A and 2B is disadvantageous in size.

[0022] In Fig. 3, which illustrates a second prior art bump leaded film carrier type semiconductor device (see: JP-A-HEI4-154136), bumps are provided instead of the outer leads of Figs. 1, 2A and 2B. That is, the conductive layers 6 are provided on the first surface S1 of the insulating film 3, and bumps 9 coupled to the conductive members 4 are provided on the second surface S2 of the insulating film 3. As a result, an area array bonding system can be adopted. Also, the device of Fig. 3 is advantageous in size.

[0023] In the device of Fig. 3, however, since the support of the chip 1 to the insulating film 3 is still carried out by only the bonding of the pads 2 to the bumps 5, the mechanical strength of the device is deteriorated.

[0024] In Fig. 4, which is a modification of the device of Fig. 3 (see: JP-A-HEI5-82586), transfer molding using resin is introduced to improve the contact characteristics of the chip 1 to the insulating film 3. That is, the chip 1 is entirely covered by resin indicated by reference numeral 10. In this case, in order to effectively transfer molding, other bumps 11 are added to the pads 2, thus enlarging a gap between the chip 1 and the insulating film 3.

[0025] In the device of Fig. 4, however, although the mechanical strength can be improved, there is a disadvantage in that the device is large in size due to the presence of resin and the enlarged gap between the chip 1 and the insulating film 3.

[0026] Fig. 5A is a cross-sectional view illustrating a first embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 5B is a bottom view of the device of Fig. 5A. Note that Fig. 5A is a cross-sectional view taken along the line A-A of Fig. 5B. In a similar way to that in Fig. 3, the conductive layers 6 are formed on the first surface S1 of the insulating film 3. On the other hand, the bumps 9 made of solder are provided on the second surface S2 of the insulating film 3. In this case, as illustrated in Fig. 5B, the bumps 9 are arranged in a grid having the same pitch, thus realizing an area array bonding system.

[0027] In Figs. 5A and 5B, the bumps 5 of Fig. 3 are not provided. Instead of this, the conductive layers 6 are connected directly to the pads 2. For realizing such direct connection of the conductive layers 6 to the pads 2, openings 21 are provided in the insulating film 3, to locally press the conductive layers 6 to the pads 2. This will be explained later.

[0028] In Figs. 5A and 5B, the chip 1 is bonded by an adhesive (tape) layer 22 to the insulating film 3, thus obtaining good contact characteristics of the chip 1 to the insulating film 3. Also, since the adhesive layer 22 can be made thin, the device of Figs. 5A and 5B can be small in size.

[0029] In Fig. 5A, note that reference numeral 2' designates a passivation layer for covering the chip 1, which is made of polyimide, silicon nitride or silicon oxide.

[0030] The manufacturing steps of the semiconductor devce of Figs. 5A and 5B are explained next with reference to Figs. 6A and 6B, 7A through 7H, and 8.

[0031] First, a film carrier 30 as illustrated in Figs. 6A and 6B is prepared. Note that Fig. 6A shows a conductive pattern side (first surface) of the film carrier 30, and Fig. 6B shows a substrate side (second surface) of the film carrier 30. That is, a conductive pattern 60 including the conductive layers 6 and test pads 601 is formed by using a photolithography and etching process on the first surface S1 of the film carrier 30. Then, the openings 21 and the through holes for the conductive members 4 are perforated by laser or etching in the film carrier 30. Then, the conductive members 4 are fitted into the through holes. In this case, the conductive members 4 are made of Au, Ni or Cu, preferably, Cu, since Au is expensive and Ni is easily cracked. Also, plating of flash gold (Au) or tin (Sn) is performed upon the conductive members 4. If gold is used, the thickness thereof is sufficiently thin, i.e., about 0.5μm to improve the erosion characteristics. Then, the film carrier 30 is perforated to form sprocket holes 301 and alignment holes 302.

[0032] Note that, the conductive members 4 can be positively protruded on the horizontal direction on the second surface S2 of the film carrier 30, to increase the land diameter of the bumps 9, thus strengthening the mechanical contact characteristics therebetween.

[0033] Next, referring to Fig. 7A, the film carrier 30 of Figs. 6A and 6B is reversed and is arranged over the chip 1 which is also reversed. In this state, the adhesive tape 22 is interposed between the film carrier 30 and the chip 1.

[0034] Next, referring to Fig. 7B, the adhesive tape 22 is set on the chip 1. In this case, the adhesive tape 22 is made of thermoplastic resin, and the adhesive tape 22 is heated from the side of the chip 1 to a melting temperature, so that the adhesive tape 22 is provisionally fixed to the chip 1. Also, the setting and heating of the adhesive tape 22 is carried out to prevent a void from being trapped therein.

[0035] In Fig. 7B, note that the adhesive tape 22 can be set on the film carrier 30.

[0036] Next, referring to Fig. 7C, a single point bonding system is used to carry out a bonding of inner leads, i.e., to bond the chip 1 to the film carrier 30. The single point bonding system using heat and ultrasonic waves has better heat transfer characteristics than a gang bonding system. That is, the Cu component of the conductive layers 6 of the conductive pattern 60 and the Al component of the pads 2 form alloy so that the conductive layers 6 are firmly bonded to the pads 2 of the chip 1.

[0037] As illustrated in Fig. 8, which is a partial enlargement of Fig. 7C, the film carrier 30 is deformed by the thickness of the adhesive tape 22, but there is no problem due to the flexibility characteristics of the film carrier 30, which is made of organic material, and the extensible characteristics of the conductive layer 6. Also, when the temperature returns to room temperature, shrinkage is generated in the film carrier 30 due to the difference in thermal expansivity between the heated temperature and the room temperature. However, the flat characteristics of the film carrier 30 is not so deteriorated as compared with a gang bonding system where the surface of the chip 1 is usually heated up to about 500°C.

[0038] In Fig. 8, note that reference numeral 23 designates a bonding tool whose weight and operational time are controlled in accordance with the width of the conductive layer 6 and the like. Also, ultrasonic waves can be used for operating the bonding tool 23.

[0039] Next, referring to Fig. 7D, in order to firmly adhere the film carrier 30 to the chip 1 with the adhesive tape 22 therebetween, a heating and pressuring operation is carried out for a few seconds from the tape side or the chip side. As a result, both of the film carrier 30 and the chip 1 are adhered to each other, and simultaneously, a component of the adhesive tape 22 is penetrated into the inner lead portions and extends to the outer periphery of the chip 1. Therefore, the adhesive tape 22 may be finally diffused into the entire chip 1. Also, sealing of an active region of the film carrier 30 and the inner lead portions, an insulation with the chip 1, and a shield effect for α-ray can be expected. Note that, even when a weight of several kg/cm^2 is applied to the entire device and the temperature is about 300°C, no adverse effects such as cracking of the chip 1 and the inner lead portions is recognized. Also, in this step, provided between the solder bump mounting face of the film carrier 30 and a mounting head (not shown) are fluorocarbon polymers or ceramic having flat characteristics, to prevent the solder bump mounting face from being contaminated.

[0040] Next, referring to Fig. 7E, a test is carried out by supplying electrical signals to the test pads 601 of the conductive pattern 60.

[0041] Next, referring to Fig. 7F, the periphery of the chip 1 is cut by using a metal die (not shown). For example, a cutting operation is carried out in view of a 100 μm edge allowance, however, it is possible to carry out a precise cutting operation by laser or dicing. Thus, the insulating film 3 is left.

[0042] Finally, referring to Fig. 7G, the bumps 9 made of solder are formed on the conductive members 4. For example, balls are formed by using a wire bonding method on a wire made by solder, and the balls are bonded on the conductive menbers 4. After that, the wire is cut so that the balls are left to form the bumps 9. Also, as bump forming material, indium capable of low temperature bonding can be used instead of solder. Further, the formation of the bumps is carried out at a step for preparing the film carrier 30 as illustrated in Figs. 6A and 6B.

[0043] Thus, the device of Figs. 5A and 5B is completed.

[0044] Additionally, referring to Fig. 7H, the device of Fig. 7G is provisionally mounted on a mounting substrate 24 by using a high precision mounter (not shown). The solder bumps 9 are aligned with lands 24a of the mounting substrate 24 by using an optical system, and a weight is applied with heating, to carry out a provisional nounting of the device. After that, a proper bonding is carried out in a reflow furnace. Also, in a case where the diameter of the solder bumps 9 and the diameter of the lands 24a are large, it is sufficient to align the bumps 9 with the lands 24a due to the self-alignment effect of solder by setting the assembly in an alignment tool and putting it in a furnace. Note that, the pitch of pads for the outer leads is preferably about 0.5 mm in view of the mounting characteristics. Also, if solder is also formed on the mounting substrate 24, it is possible to increase the distance between the insulating film 3 and the substrate 24.

[0045] Also, at the step as illustrated in Fig. 7G, it is possible to fit fillers made of resin into the openings 21.

[0046] Fig. 9A is a cross-sectional view illustrating a second embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 9B is a bottom view of the device of Fig. 9A. Note that Fig. 9A is a cross-sectional view taken along the line A-A of Fig. 9B. In Figs. 9A and 9B, through holes 31 are provided in the insulating film 3 instead of the openings 21 of Figs. 5A and 5B. Fillers 32 made of metal are fitted into the through holes 31. Therefore, when bonding inner leads by a bonding tool, the bonding tool can easily push each of the conductive layers 6 via a respective one of the fillers 32. Also, the through hole 31 can be precisely formed in alignment with the pads 2 of the chip 1 and the conductive layers 6. Further, the

mechanical strength in the inner lead portions can be strengthened. Still further, since energy is transmitted effectively from the fillers 32 to the inner lead portions, the bonding condition of the inner leads can be relaxed.

[0047] The manufacturing steps of the semiconductor device of Figs. 9A and 9B are explained next with reference to Figs. 10A and 10B, 11A through 11H, and 12, which correspond to Figs. 6A and 6B, 7A through 7H, and 8, respectively.

[0048] As shown in Figs. 10A and 10B, the through holes 31 and the fillers 32 therein are provided instead of the openings 21 of Figs. 6A and 6B. In this case, the through holes 31 formed by laser or an etching process have to be in alignment with the conductive layers 6. For example, if the pads 2 are arranged at a pitch of 100μm on the chip 1, the pitch of the through holes 31 is also 100μm. Also, the width of the conductive layers 6 is as large as possible in view of the alignment with the through holes 31. On the other hand, the width of the conductive layers 6 is as small as possible in view of the prevention of short circuits around the conductive member 4 (or the bumps 9) in a grid. For example, if the width of the conductive layers 6 is about 70 μm, the through holes 31 are 50 μm in diameter. Also, in order to precisely form the through holes 31, the film carrier 30 is as thin as possible.

[0049] In the manufacturing steps as shown in Figs. 11A through 11H, a single point bonding system is adopted, which is different from those as shown in Figs. 7A through 7H. The single point bonding system is shown in detail in Figs. 11C and 12. That is, a bonding tool 23 is provided for each of the fillers 32, i.e., each of the conductive layers 6. Also, in this case, the surface of the chip 1 is heated up to about 300 °C.

[0050] Fig. 13A is a cross-sectional view illustrating a third embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 13B is a bottom view of the device of Fig. 13A. Note that Fig. 13A is a cross-sectional view taken along the line A-A of Fig. 13B. In Figs. 13A and 13B, fillers 42 made of metal are inserted between the pads 2 and the conductive layers 6, to easily push the conductive layers 6 by the bonding tool 23' (see Fig. 12). Also, the metal fillers 42 can be easily formed by solder bumps using a solder bump system. Therefore, the metal fillers 42 are advantageous in shear strength as compared with the parts 6a of the conductive layers 6 of the third embodiment.

[0051] Fig. 14A is a cross-sectional view illustrating a fourth embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 14B is a bottom view of the device of Fig. 14A. Note that Fig. 14A is a cross-sectional view taken along the line A-A of Fig. 14B. The fourth embodiment is similar to the third embodiment. That is, in Figs. 14A and 14B, metal fillers 43 are positively protruded along the horizontal direction on the first surface S1 of the insulating film 3. As a result, the thickness of the insulating film 3 can be reduced more in the fourth embodiment than in the third embodiment, thus reducing the device in size.

[0052] Figs. 15A and 15B show a film carrier 30 used for manufacturing the devices of Figs. 13A, 13B and 14A, 14B. In this case, Fig. 15A shows a chip side surface (first surface) of the film carrier 30, and Fig. 15B shows a conductive pattern side (second surface) of the film carrier 30. Since the conductive layers 6 are located on the second surface S2 of the film carrier 30, the cover 41 covers the conductive layers 6 except for the inner lead portions and the test pads 601 thereof, which is different from the film carriers as shown in Figs. 5A, 5B, 10A and 10B.

[0053] In the above-described embodiments, the adhesive (tape) layer 22 can be made of thermosetting resin or thermoplastic resin. Thermoplastic polyimide is polymer coupled by imide coupling of aromatic molecules, so that a heat resistance of higher than 400°C is obtained. Also, the mutual interruption of molecules of the thermoplastic resin is weak, and therefore, the thermoplastic resin has thermal flowability. Also, the glass transition temperature of the thermoplastic resin for defining the thermal flowability can be arbitrarily controlled. Thus, thermoplastic resin rather than thermosetting resin is preferable for the adhesive (tape) layer 22. Further, since a bonding between the chip 1 and the insulating film 3 is carried out at a low temperature and a low pressure, thermoplastic resin is preferable. However, other heat-resistant adhesive film and thermosetting polyimide capable of high speed curing can be used as the adhesive (tape) layer 22.

[0054] On the other hand, organic material of the adhesive layer 22 is adhered to conductive portions such as the pads 2 and the conductive layers 6, thus deteriorating the reliability. To avoid this, the size of the adhesive layer 22 should be smaller than that of the chip 1. Also, the adhesive layer 22 is as thin as possible, to reduce a step between the chip 1 and the insulating film 3. For example, the adhesive layer 22 is preferably about 10 to 30 μm.

[0055] Thus, according to the first to fifth embodiments, since the flexible insulating film 3 is interposed between the chip 1 and the substrate 24, a stress generated due to the difference in thermal expansibility rate therebetween can be relaxed. In the prior art flip-chip bonding system, a height of about 100 μm is required and insertion of liquid resin into gaps is indispensible, while, in the above-described embodiments, since the height after bonding can be smaller than about 50 μm, the diameter of the bumps 9 can be smaller than about 80 μm in diameter in view of the warpage of the substrate 24. Also, even when the device is mounted without resin sealing on a printed substrate having a large difference in thermal extensibility rate, it is possible to pass a temperature cycle test (300 cycles of -25°C/30 minutes and 125°C/30 minutes). Further, since the film carrier 30 and the adhesive layer 22 serve as a cover

against solder flux, the residual flux left by insufficient cleaning can be compensated for.

[0056] Fig. 16A is a cross-sectional view illustrating a fifth embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 16B is a bottom view of the device of Fig. 16A. Note that Fig. 16A is a cross-sectional view taken along the line A-A of Fig. 16B. In Figs. 16A and 16B, a resin injection opening 3a is perforated at a center of the insulating film 3 of Figs. 9A and 9B. That is, liquid resin is injected via the resin injection opening 3a into a gap between the chip 1 and the insulating film 3, to thereby form a resin layer 51 instead of the adhesive layer 22 of Figs. 9A and 9B.

[0057] The manufacturing steps of the semiconductor device of Figs. 16A and 16B are explained next with reference to Figs. 17A through 17G which correspond to Figs. 11A, 11C through 11H, respectively.

[0058] First, referring to Fig. 17A, in a similar way as that in Fig. 11A, the film carrier 30 similar to that as shown in Figs. 6A and 6B except for the resin injection opening 3a is reversed and is arranged over the chip 1 which is also reversed.

[0059] Next, referring to Fig. 17B, in the same way as in Fig. 11C, a single point bonding system is used to carry out a bonding of inner leads, i.e., to bond the chip 1 to the film carrier 30.

[0060] Next, referring to Fig. 17C, resin for sealing is injected via the resin injection opening 51 into a gap between the chip 1 and the film carrier 30, to form the resin layer 51. In this case, this resin is preferably one having a suitable flowability and is capable of forming a thin coating film. Although epoxy, silicon, silicon epoxy, fluorocarbon polymers and the like are considered as such a resin, silicon and fluorocarbon polymers are preferable due to their rubber characteristics after curing. Further, in order to reduce the shrinkage of the film carrier 30 and obtain high flat characteristics, curing is carried out after a light homogenity operation is carried out. Although the flat characteristics, the homogeneous coating amount, and control of regions are reduced as compared with the second embodiment of the manufacturing method, it is possible to easily spill resin from the surface of the chip 1. That is, as will be stated later, although it is considered that the periphery of the chip 1 is again sealed with liquid resin in accordance with a requested level of the reliablity, particularly, the humidity resistance characteristics, it is possible to simultaneously carry this out.

[0061] The manufacturing steps as shown in Figs. 17D through 17G are the same as those as shown in Figs. 11E through 11H.

[0062] Note that, the semiconductor device of the second embodiment is modified and is applied to the fifth embodiment; however, the first, third or fourth embodiment can be modified and applied to the fifth embodiment.

[0063] Also, although the fifth embodiment is similar to the prior art as shown in Fig. 4, in this prior art, resin is injected into the gap between the chip 1 and the insulating film 3 from the sides thereof, with difficulty, while, in the fifth embodiment, resin is easily injected into the gap between the chip 1 and the insulating film 3 from the center thereof.

[0064] In Fig. 18A, which is a cross-sectional view illustrating a sixth embodiment of the bump leaded film carrier type semiconductor device according to the present invention, a step for sealing the periphery of the chip 1 with liquid resin 52 by potting is added, thus improving the humidity resistance. In this case, the back face of the chip 1 is not sealed in Fig. 18. Therefore, a heat spreader or a heat sink is adhered to the back face, to thereby improve heat dissipation characteristics. Such a sealing step is inserted between the steps as shown in Figs. 11D and 11E. In this case, low stress, no void, contact characteristics and crack characteristics for solder are necessary. Also, a margin of about 0.5 mm at each side of the chip 1 and a margin of about 0.1 mm in a thickness direction of the chip 1 are required generally as sizes for easy manufacture. Note that, since sealing between the chip 1 and the film carrier 30 is already carried out, only the outside of the chip 1 is required to be immersed in resin.

[0065] Even in the sixth embodiment, the semiconductor device of the second embodiment is modified and is applied to the sixth embodiment; however, the first, third or fourth embodiment can be modified and applied to the sixth embodiment.

[0066] Fig. 19A and 19B are cross-sectional views illustrating a seventh embodiment of the bump leaded film carrier type semiconductor device according to the present invention, and Fig. 19C is a bottom view of the device of Fig. 19A and 19B. Note that Figs. 19A and 19B are cross-sectional views taken along the line A-A and the like B-B, respectively of Fig. 19C. In Figs. 19A, 19B and 19C, the sides and back face of the chip 1 are covered by a resin layer 53. Particularly, conductive bumps 9' for outer leads are also provided on the insulating film 3 outside of the chip 1. Assume that the outer lead bumps 9, whose pitch is 0.5 mm, are arranged in a grid, then it is possible to arrange more bumps 9 than 226 in a chip mounting area of 7 mm square. In this case, the outer lead bumps 9' outside of the chip 1 are helpful in the enhancement of the integration while retaining the flat characteristics.

[0067] The manufacturing steps of the semiconductor device of Figs. 19A, 19B and 19C are the same as those of Figs. 11A through 11H except that a transfer molding step is added after the step as shown in Fig. 11E. In the transfer molding step, the device of Figs. 11E is mounted on a lower metal mold, and then an upper metal mold is lowered to sandwich the device of Fig. 11E between the upper and lower metal molds. Then, heated resin is injected from a pot via a runner and a gate into a gap (cavity) within the metal molds. Provisional curing is carried out for several minutes. After that, the metal molds

are taken out of the resin molded device. Then, final curing is carried out at a temperature of 170 to 180°C for a couple of hours.

[0068] Note that, the semiconductor device of the second embodiment is modified and is applied to the seventh embodiment; however, the first, third or fourth embodiment can be modified and applied to the seventh embodiment.

[0069] As explained hereinbefore, according to the present invention, since use is made of an adhesive (tape) layer between a chip and an insulating film or resin injected from a center of the insulating film, the bump leaded semiconductor device of the present invention can be firm and small in size.

Claims

1. A method for manufacturing a semiconductor device, comprising the steps of:

   preparing an insulating film (3) having a first surface (S1) on which conductive layers (6) are formed and having openings (21, 31) therethrough, said opening covered with respective ones of said conductive layers;

   preparing a semiconductor chip (1) having pads (2) each located to oppose respective ones of said openings and a passivation film (2') located so that said pads are surrounded by said passivation film;

   adhering said semiconductor chip to said first surface (S1) of said insulating film (3) by an adhesive layer so that said openings oppose respective ones of said pads via respective ones of said conductive layers; and

   locally bending said conductive layers by inserting a bonding tool (23) into said openings and pressing said conductive layers with said bonding tool, thereby electrically connecting said conductive layers with said respective ones of said pads.

2. A method as set forth in claim 1, further comprising a step of forming conductive protrusions (9) on a second surface (S2) of said insulating film, said conductive protrusions being connected through said insulating film to respective ones of said conductive layers.

3. A method as set forth in claim 2, wherein conductive members (4) are inserted into through holes provided in said insulating film to electrically connect said conductive protrusions to respective ones of said conductive layers.

4. A method as set forth in claim 2, wherein a filler (32) is fitted into each of said openings.

5. A method as set forth in claim 2, further comprising a step of potting only sides of said semiconductor device by resin after said local pressing step is completed.

6. A method as set forth in claim 2, further comprising a step of transfer-molding said semiconductor device after said local pressing step is completed.

7. A method for manufacturing a semiconductor device, comprising the steps of:

   preparing an insulating film (3) having a first surface (S1) on which conductive layers (6) are formed and having openings (21, 31) therethrough, said opening covered with respective ones of said conductive layers;

   preparing a semiconductor chip (1) having pads (2) each located to oppose respective ones of said openings and a passivation film (2') located so that said pads are surrounded by said passivation film;

   positioning said chip to said first surface (S1) of said insulating film (3) so that said openings oppose respective ones of said pads via respective ones of said conductive layers;

   locally bending said conductive layers by inserting a bonding tool (23) into said openings and pressing said conductive layers with said bonding tool, thereby electrically connecting said conductive layers with said respective ones of said pads and bonding said chip to said conductive layers; and

   said insulating film has a resin injection opening (3a) at a center portion thereof, said method further comprising a step of injecting resin via said resin injection opening into a gap between said insulating film and said semiconductor chip.

8. A method for manufacturing a semiconductor device, comprising the steps of:

   preparing an insulating film (3) having first and second surfaces (S1, S2) and through holes (31) therethrough, conductive layers (6) being formed on said second surface, conductive protrusions (9) being formed on said conductive layers, metal fillers (42, 43) being formed in said through holes and being connected to respective ones of said conductive layers;

adhering a semiconductor chip (1) having pads (2) to said first surface (S1) of said insulating film by an adhesive layer (22) so that said metal fillers oppose respective ones of said pads; and

locally bending and pressing said conductive layers so that said conductive layers are electrically connected via said metal fillers to said respective ones of said pads.

9. A method as set forth in claim 8, wherein said metal fillers (43) protrude further than said conductive layers (6) from said first surface (S1) of said insulating film.

10. A method as set forth in claim 8, further comprising a step of potting only sides of said semiconductor device by resin after said local pressing step is completed.

11. A method as set forth in claim 8, further comprising a step of transfer-molding said semiconductor device after said local pressing step is completed.

Patentansprüche

1. Verfahren zum Herstellen einer Halbleitervorrichtung, das die folgenden Schritte aufweist:

Herstellen einer Isolationsschicht (3), die eine erste Oberfläche (S1), auf der leitende Schichten (6) ausgebildet werden, und die durchgehende Öffnungen (21, 31) hat, wobei die Öffnungen mit jeweiligen, leitenden Schichten abgedeckt sind;

Herstellen eines Halbleiterchips (1), der Kontaktabschnitte (2), von denen jeder gegenüber einer jeweiligen der Öffnungen angeordnet ist, und eine Passivierungsschicht (2') hat, die derart angeordnet ist, dass die Kontaktabschnitte von der Passivierungsschicht umgeben sind;

Aufkleben des Halbleiterchips auf die erste Oberfläche (S1) der Isolationsschicht (3) durch eine Klebeschicht derart, dass die Öffnungen gegenüber jeweiligen Kontaktabschnitten über jeweilige, leitende Schichten sind; und

örtliches Biegen der leitenden Schichten durch Einfügen eines Bondwerkzeugs (23) in die Öffnungen und durch Pressen der leitenden Schichten mit dem Bondwerkzeug, wodurch die leitenden Schichten mit den jeweiligen Kontaktabschnitten elektrisch verbunden werden.

2. Verfahren nach Anspruch 1, das weiterhin einen Schritt zum Ausbilden von leitenden Vorsprüngen (9) an einer zweiten Oberfläche (S2) der Isolationsschicht aufweist, wobei die leitenden Vorsprünge durch die Isolationsschicht mit jeweiligen, leitenden Schichten verbunden sind.

3. Verfahren nach Anspruch 2, worin leitende Teile (4) in Durchgangslöcher eingesetzt werden, die in der Isolationsschicht vorgesehen sind, um die leitenden Vorsprünge mit jeweiligen, leitenden Schichten elektrisch zu verbinden.

4. Verfahren nach Anspruch 2, worin ein Füllteil (32) in jede der Öffnungen eingesetzt wird.

5. Verfahren nach Anspruch 2, das weiterhin einen Schritt des Einbettens nur der Seiten der Halbleitervorrichtung in Kunststoff bzw. Harz aufweist, nachdem der lokale Pressschritt beendet worden ist.

6. Verfahren nach Anspruch 2, das weiterhin einen Schritt des Pressgießens der Halbleitervorrichtung aufweist, nachdem der lokale Pressschritt abgeschlossen worden ist.

7. Verfahren zum Herstellen einer Halbleitervorrichtung, das die folgenden Schritte aufweist:

Herstellen einer Isolationsschicht (3), die eine erste Oberfläche (S1), auf der leitende Schichten (6) ausgebildet werden, und die durchgehende Öffnungen (21, 31) hat, wobei die Öffnungen mit jeweiligen, leitenden Schichten abgedeckt sind;

Herstellen eines Halbleiterchips (1), der Kontaktabschnitte (2), die jeweils gegenüber einer jeweiligen der Öffnungen angeordnet sind, und eine Passivierungsschicht (2') hat, die derart angeordnet ist, dass die Kontaktabschnitte von der Passivierungsschicht umgeben sind;

Positionieren des Chips gegenüber der ersten Oberfläche (S1) der Isolationsschicht (3) derart, dass die Öffnungen gegenüber jeweiligen Kontaktabschnitten über jeweilige, leitende Schichten sind;

örtliches Biegen der leitenden Schichten durch Einsetzen eines Bondwerkzeugs (23) in die Öffnungen und durch Pressen der leitenden Schichten mit dem Bondwerkzeug, wodurch die leitenden Schichten mit jeweiligen Kontaktabschnitten elektrisch verbunden werden und der Chip mit den leitenden Schichten verbunden wird; und

wobei die Isolationsschicht eine Kunststoffin-

jektionsöffnung (3a) in einem Mittenabschnitt davon hat und wobei das Verfahren weiterhin einen Schritt des Injizierens von Kunststoff bzw. Harz über die Kunststoffinjektionsöffnung in einen Spalt zwischen der Isolationsschicht und dem Halbleiterchip aufweist.

8. Verfahren zum Herstellen einer Halbleitervorrichtung, das die folgenden Schritte aufweist:

Herstellen einer Isolationsschicht (3), die eine erste Oberfläche und eine zweite Oberfläche (S1, S2) und Durchgangslöcher (31) durch sie hindurch hat, leitender Schichten (6), die auf der zweiten Oberfläche ausgebildet sind, leitender Vorsprünge (9), die auf den leitenden Schichten ausgebildet sind, und von Metallfüllteilen (42, 43), die in den Durchgangslöchern ausgebildet sind und die mit jeweiligen, leitenden Schichten verbunden sind;

Aufkleben eines Halbleiterchips (1) mit Kontaktabschnitten (2) auf die erste Oberfläche (S1) der Isolationsschicht mittels einer Klebeschicht (22) derart, dass die Metallfüllteile jeweiligen Kontaktabschnitten gegenüber stehen; und

örtliches Biegen und Pressen der leitenden Schichten derart, dass die leitenden Schichten über die Metallfüllteile mit den jeweiligen Anschlussabschnitten elektrisch verbunden sind.

9. Verfahren nach Anspruch 8, worin die Metallfüllteile (43) weiter als die leitenden Schichten (6) von der ersten Oberfläche (S1) der Isolationsschicht hervorstehen.

10. Verfahren nach Anspruch 8, das weiterhin einen Schritt des Einbettens nur der Seiten der Halbleitervorrichtung in Kunststoff bzw. Harz aufweist, nachdem der örtliche Pressschritt abgeschlossen worden ist.

11. Verfahren nach Anspruch 8, das weiterhin einen Schritt des Pressgießens der Halbleitervorrichtung aufweist, nachdem der örtliche Pressschritt abgeschlossen worden ist.

Revendications

1. Une méthode pour fabriquer un dispositif semi-conducteur, qui comprend les étapes de:

préparer un film isolant (3) ayant une première surface (S1) sur laquelle des couches conductrices (66) soient formées et ayant des ouvertures (21, 31) à travers de celle-ci, l'ouverture étant couverte respectivement desdites couches conductrices;

préparer une puce semi-conductrice (1) ayant des coussins (2) chacun étant positionné afin d'opposer lesdites ouvertures respectives et un film de passivation (2 ') étant positionné afin que lesdits coussins soient entourés dudit film de passivation;

adhérer ladite puce semi-conductrice à ladite première surface (S1) dudit film isolant (3) par une couche adhésive afin que lesdites ouvertures opposent celles respectives desdits coussins par celles respectives desdites couches conductrices; et

courber localement lesdites couches conductrices en insérant un outil de liaison (23) dans lesdites ouvertures et en pressant lesdites couches conductrices avec ledit outil de liaison, connectant électriquement de cette façon lesdites couches conductrices avec celles respectives desdits coussins.

2. Une méthode selon la revendication 1, qui comprend en outre une étape de formation de saillies conductrices (9) sur une deuxième surface (S2) dudit film isolant, lesdites saillies conductrices étant connectées à travers ledit film isolant à celles respectives desdites couches conductrices.

3. Une méthode selon la revendication 2, où des membres conducteurs (4) sont insérés dans des trous de passage pourvus dans ledit film isolant pour connecter électriquement lesdites saillies conductrices à celles respectives desdites couches conductrices.

4. Une méthode selon la revendication 2, où une matière de remplissage (32) soit insérée dans chacune desdites ouvertures.

5. Une méthode selon la revendication 2, qui comprend en outre une étape de mise en pot seulement les côtés dudit dispositif semi-conducteur par la résine après que ladite étape de pressage local soit terminé.

6. Une méthode selon la revendication 2, qui comprend en outre une étape de moulage par transfert dudit dispositif semi-conducteur après que ladite étape de pressage local soit terminé.

7. Une méthode pour fabriquer un dispositif semi-conducteur, qui comprend les étapes de:

préparer un film isolant (3) ayant une première surface (S1) sur laquelle des couches conductrices (66) soient formées et ayant des ouvertures (21, 31) à travers de celle-ci, l'ouverture étant couverte respectivement desdites couches conductrices;

préparer une puce semi-conductrice (1) ayant des coussins (2) chacun étant positionné afin d'opposer lesdites ouvertures respectives et un film de passivation (2 ') étant positionné afin que lesdits coussins soient entourés dudit film de passivation;

positionner ladite puce à ladite première surface (S1) dudit film isolant (3) afin que lesdites ouvertures opposent celles respectives desdits coussins par celles respectives desdites couches conductrices ;

courber localement lesdites couches conductrices en insérant un outil de liaison (23) dans lesdites ouvertures et en pressant lesdites couches conductrices avec ledit outil de liaison, connectant électriquement de cette façon lesdites couches conductrices avec celles respectives desdits coussins et liant ladite puce aux dites couches conductrices et ;

ledit film isolant a une ouverture pour l'injection de la résine (3a) à une portion centrale de celui-ci, ladite méthode comprenant en outre une étape d'injection de la résine par ladite ouverture pour l'injection de la résine dans un vide entre ledit film isolant et ladite puce semi-conductrice.

8. Une méthode pour fabriquer un dispositif semi-conducteur, qui comprend les étapes de:

préparer un film isolant (3) ayant une première et une deuxième surface (S1, S2) et des trous de passage(31) à travers ceux-ci, des couches conductrices (6) étant formés sur ladite deuxième surface, des saillies conductrices (9) étant formées sur lesdites couches conductrices, des matières de remplissage métalliques (42, 43) étant formés dans lesdits trous de passage et étant connectés à ceux respectifs desdites couches conductrices;

adhérer une puce semi-conductrice (1) ayant des coussins (2) à ladite première surface (S1) dudit film isolant par une couche adhésive (22) afin que lesdites matières de remplissage métalliques opposent celles respectives desdits coussins; et

courber et presser localement lesdites couches conductrices afin que lesdites couches conductrices soient connectées électriquement par lesdites matières de remplissage métalliques respectives desdits coussins.

9. Une méthode selon la revendication 8, où lesdites matières de remplissage métalliques (43) saillissent plus que lesdites couches conductrices (6) de ladite première surface (S1) dudit film isolant.

10. Une méthode selon la revendication 2, qui comprend en outre une étape de mise en pot seulement les côtés dudit dispositif semi-conducteur par la résine après que ladite étape de pressage local soit terminé.

11. Une méthode selon la revendication 2, qui comprend en outre une étape de moulage par transfert dudit dispositif semi-conducteur après que ladite étape de pressage local soit terminé.

Flg. 1 PRIOR ART

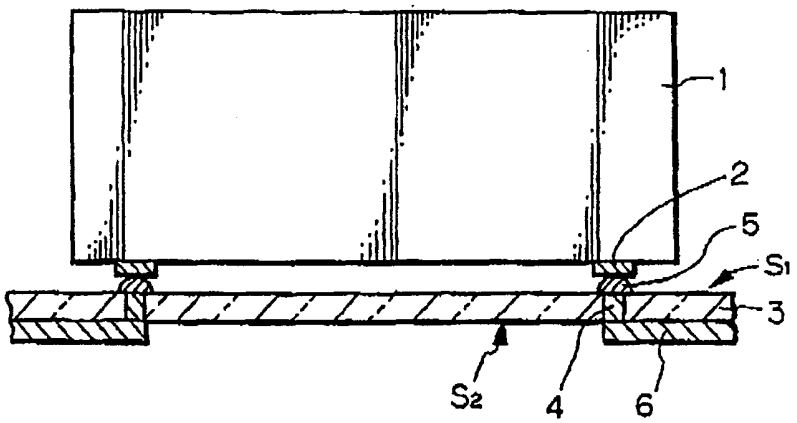


Fig. 2A PRIOR ART

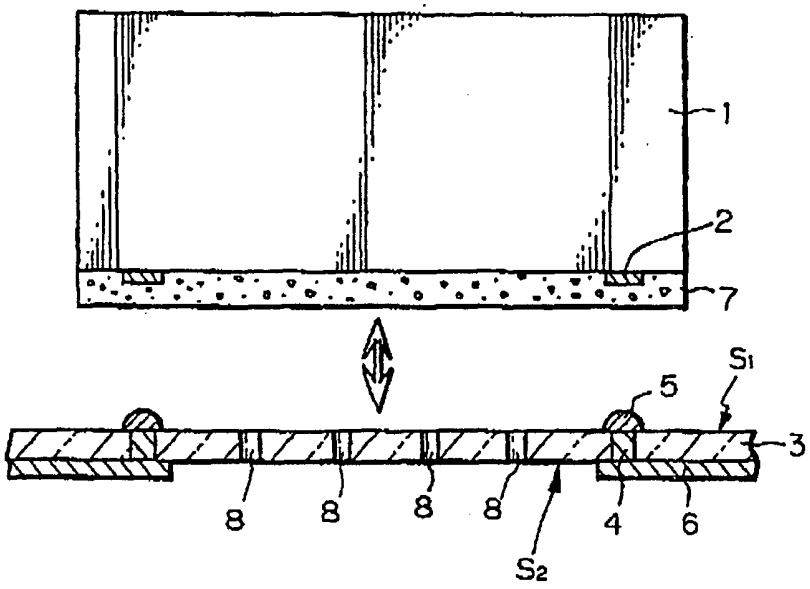


Fig. 2B PRIOR ART

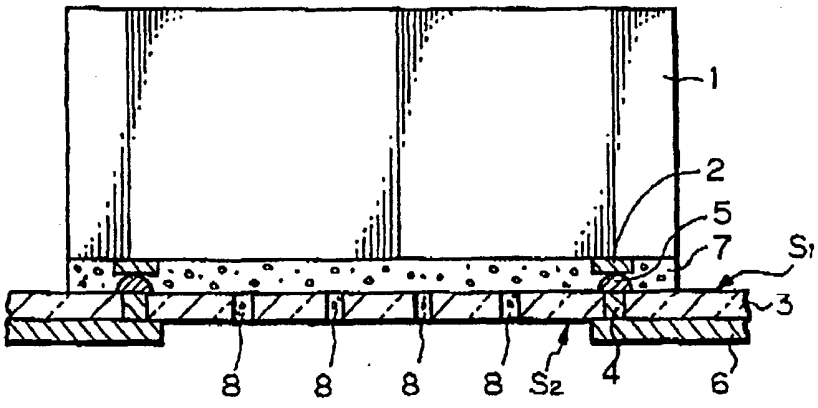


Fig. 3 PRIOR ART

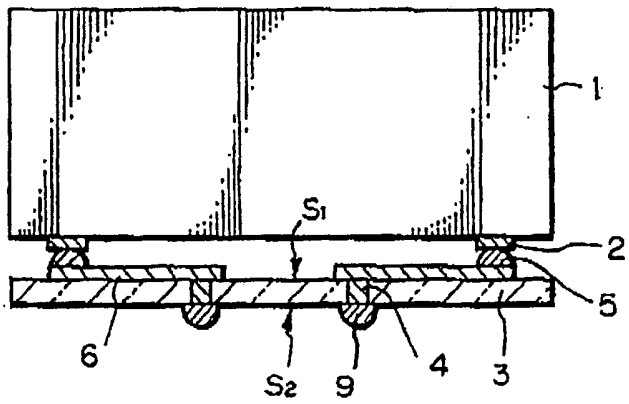


Fig. 4 PRIOR ART

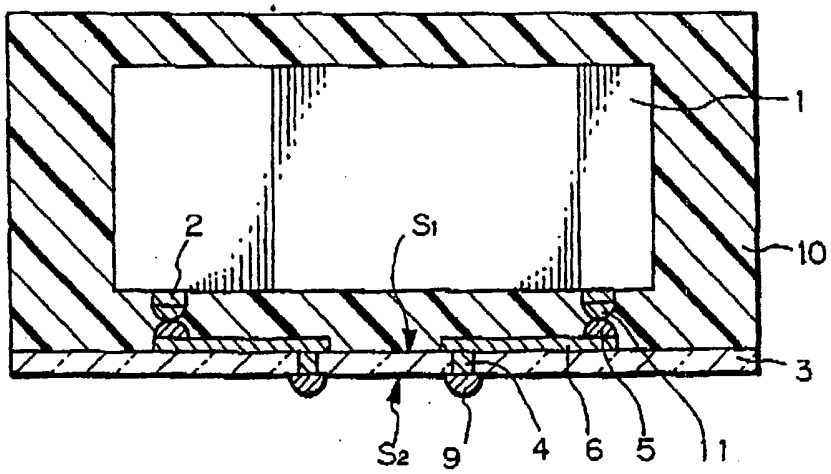


Fig. 5A

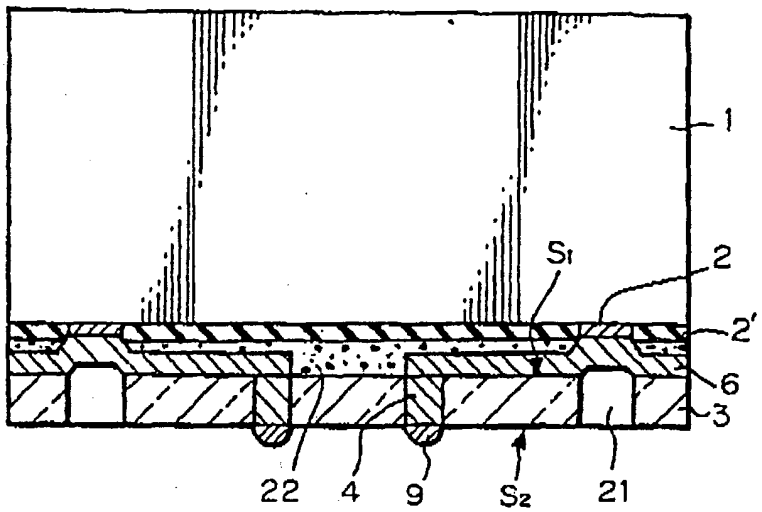


Fig. 5B

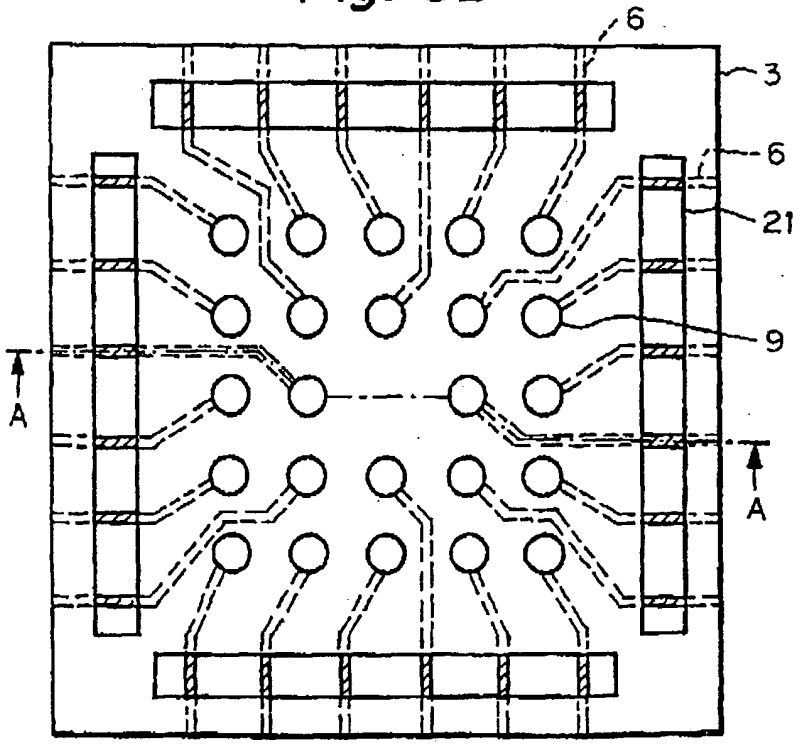


Fig. 6A

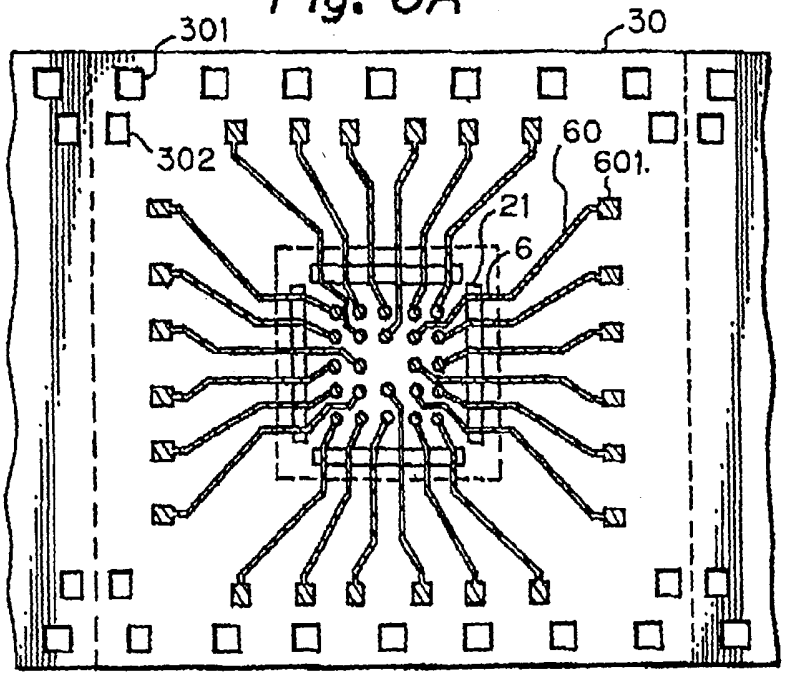


Fig. 6B

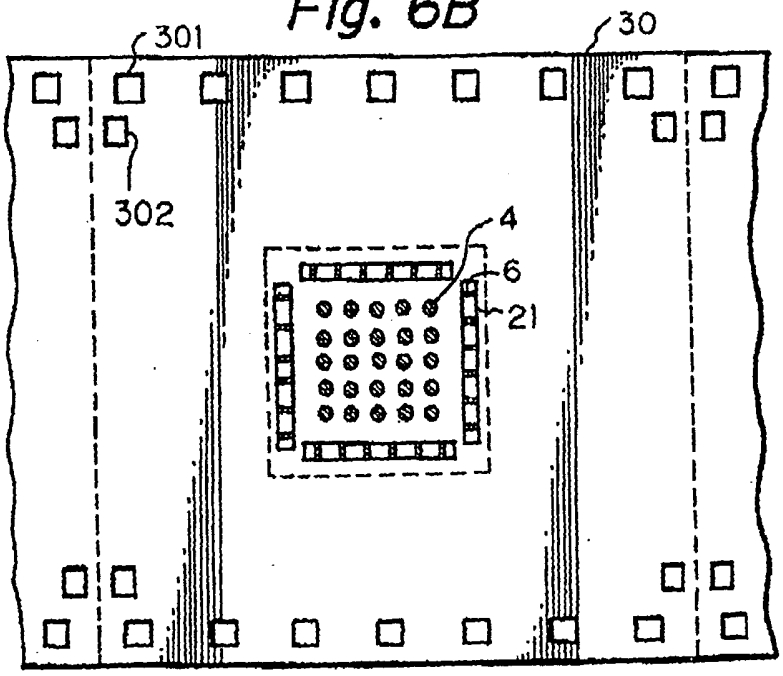


Fig. 7A

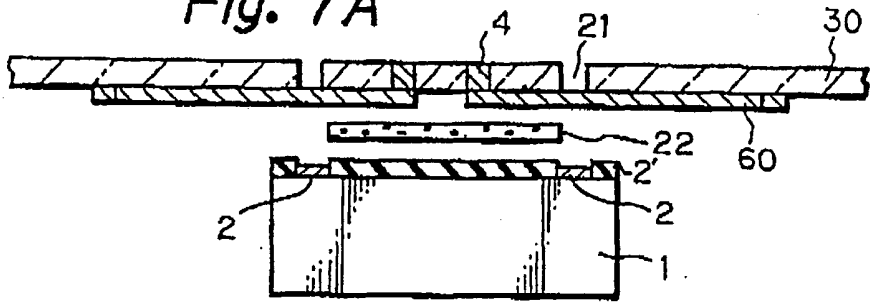


Fig. 7B

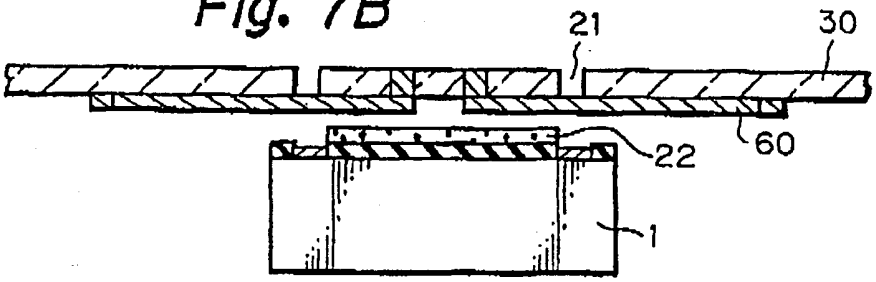


Fig. 7C

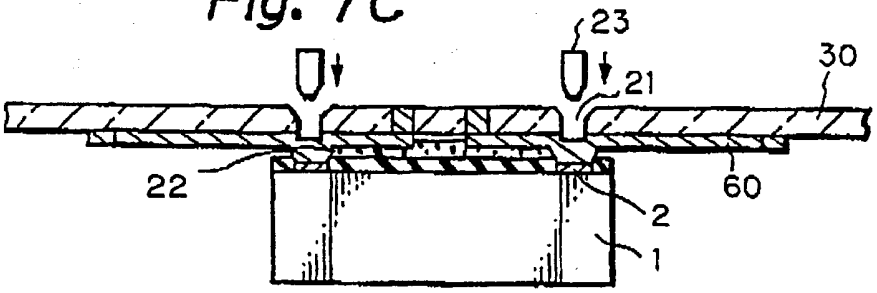


Fig. 7D

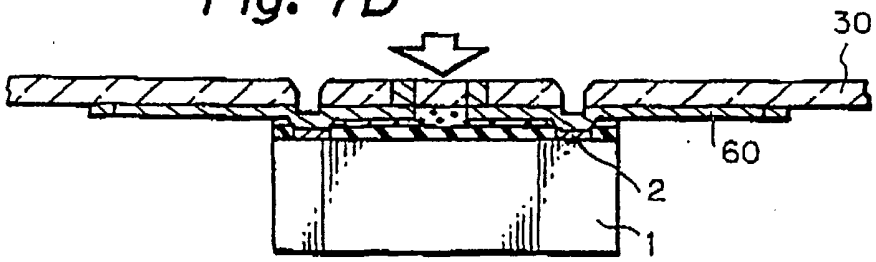


Fig. 7E

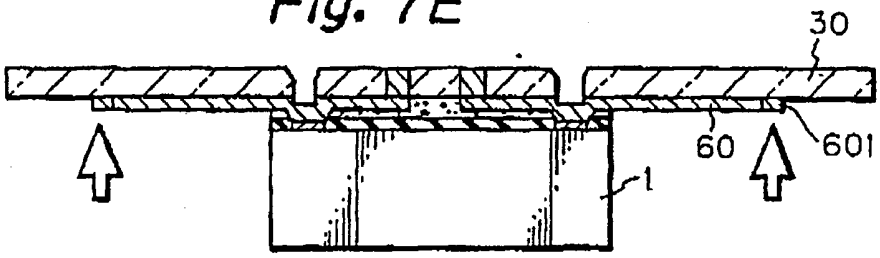


Fig. 7F

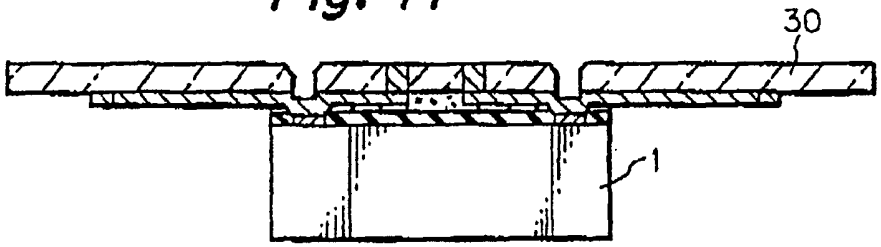


Fig. 7G

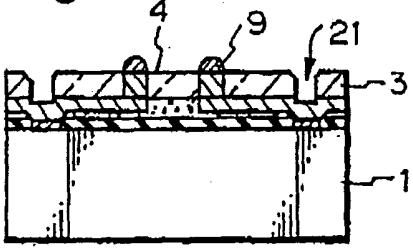


Fig. 7H

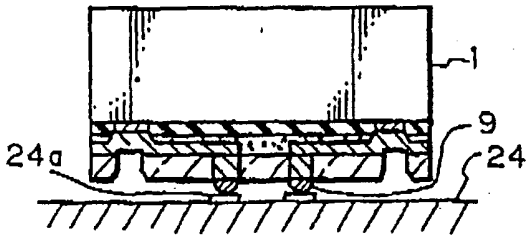


Fig. 8

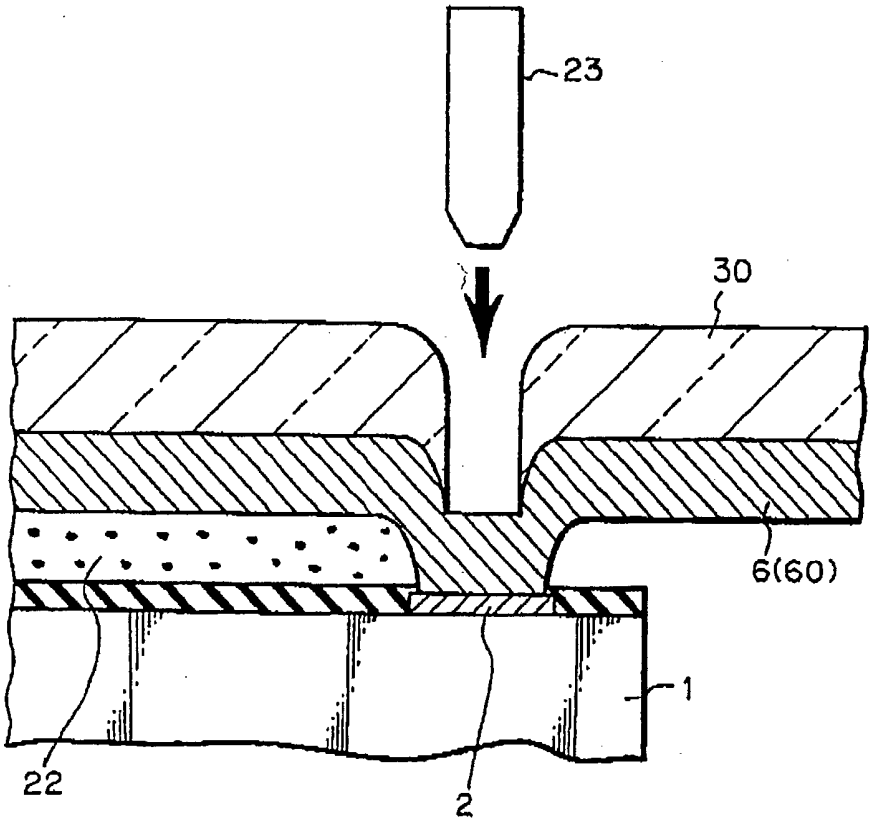


Fig. 9A

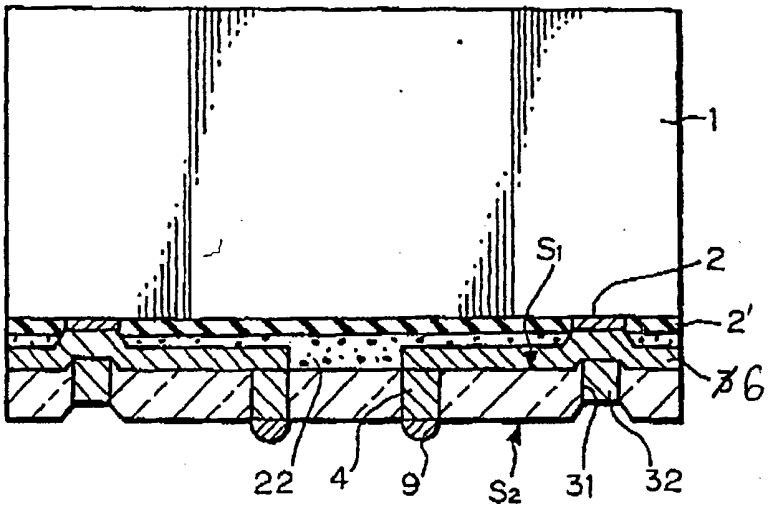


Fig. 9B

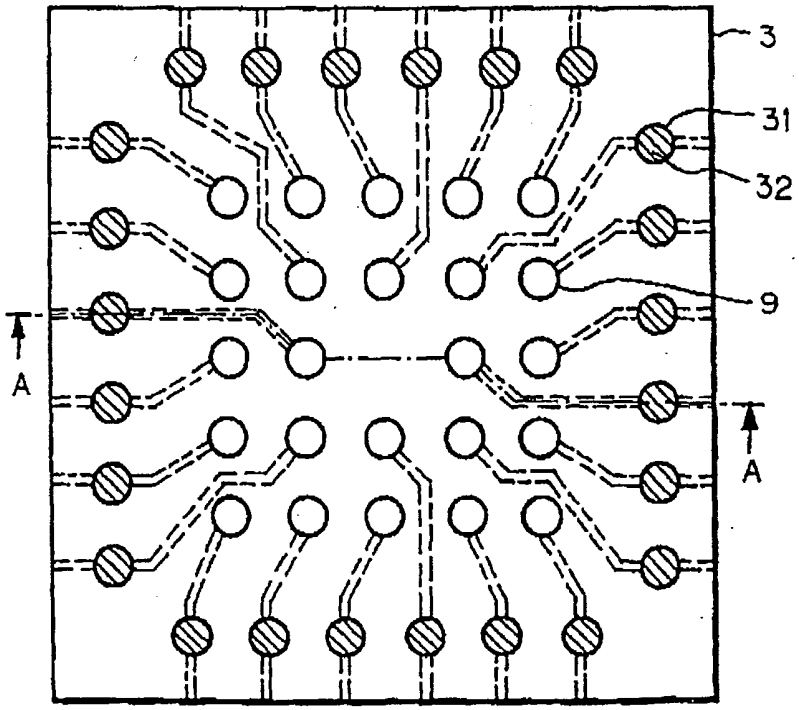


Fig. 10A

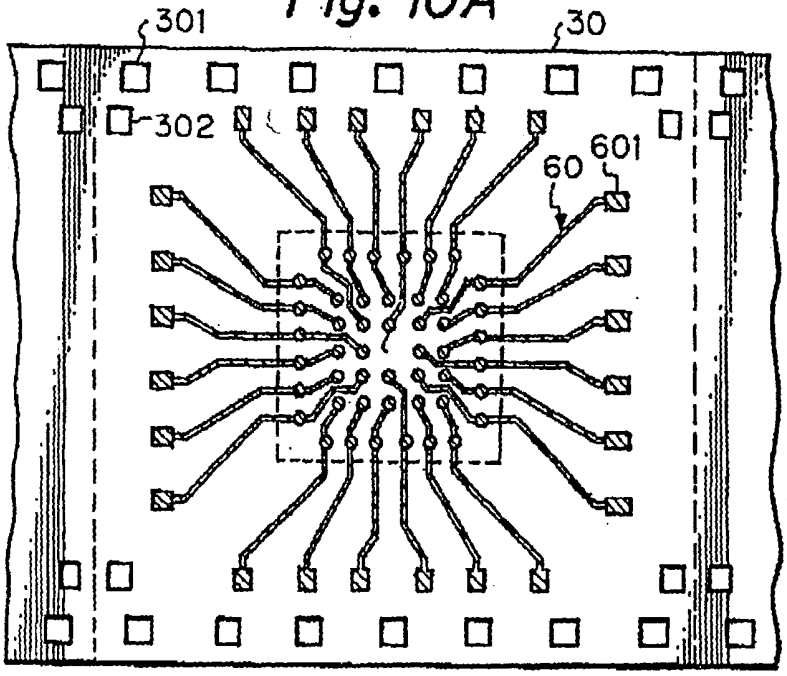


Fig. 10B

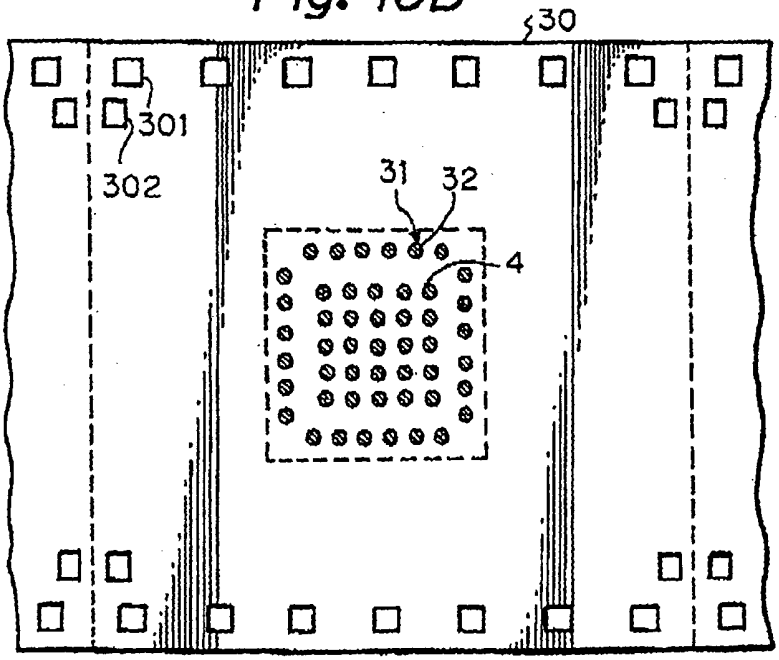


Fig. 11A

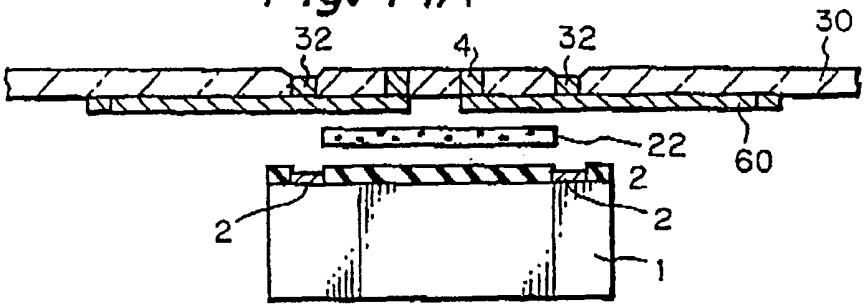


Fig. 11B

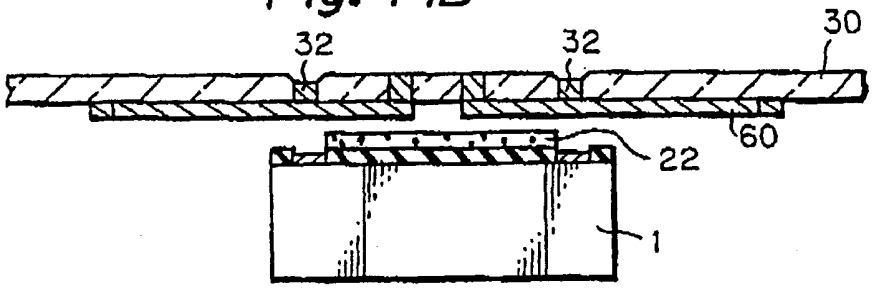


Fig. 11C

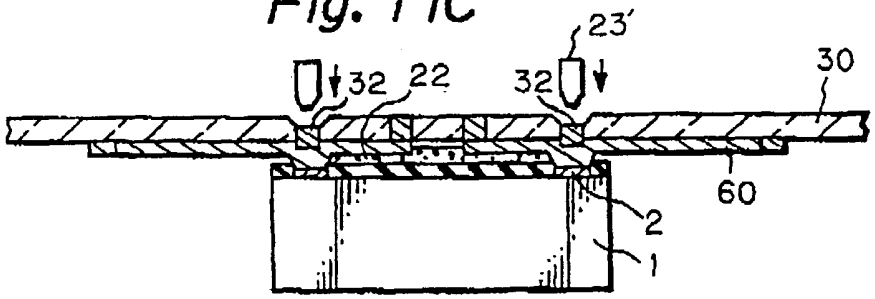


Fig. 11D

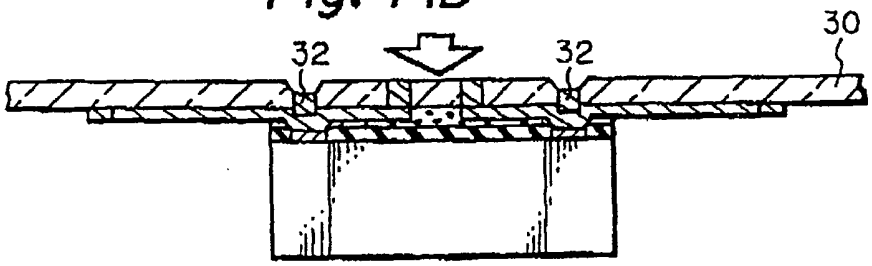


Fig. 11E

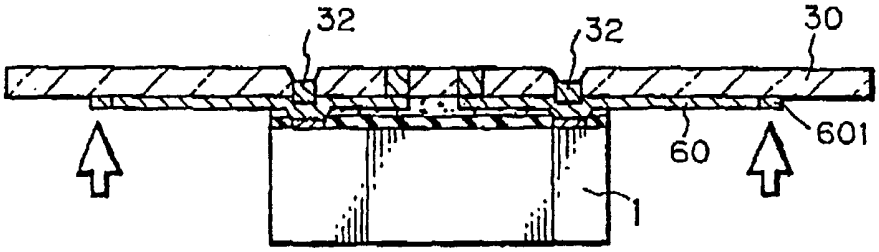


Fig. 11F

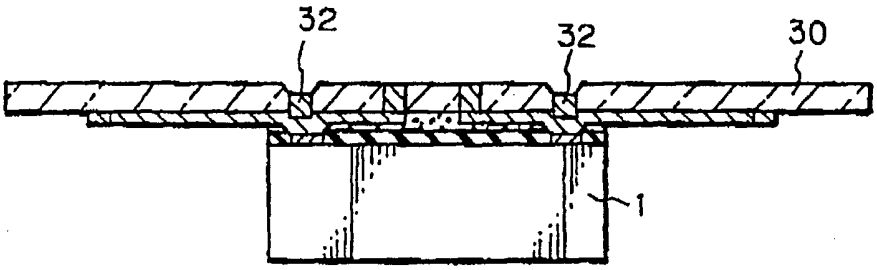


Fig. 11G

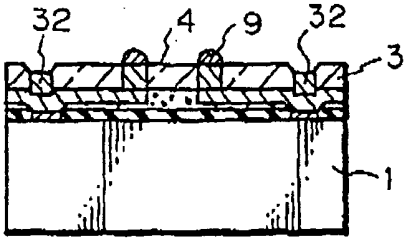
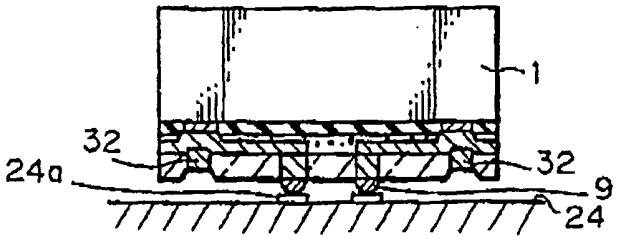


Fig. 11H



Flg. 12

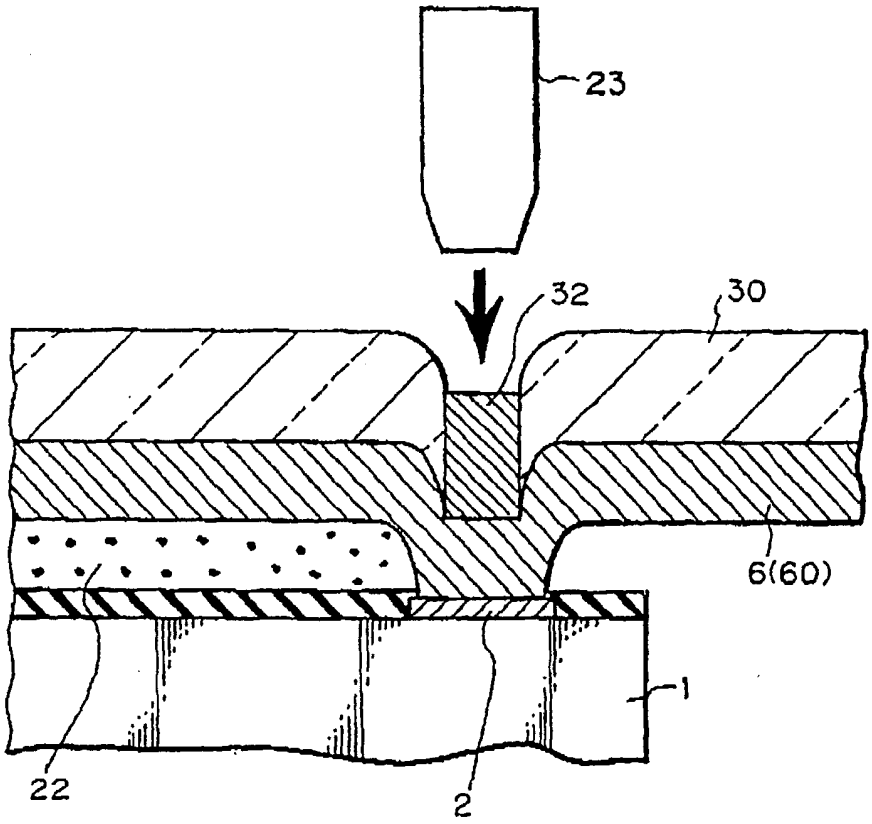


Fig. 13A

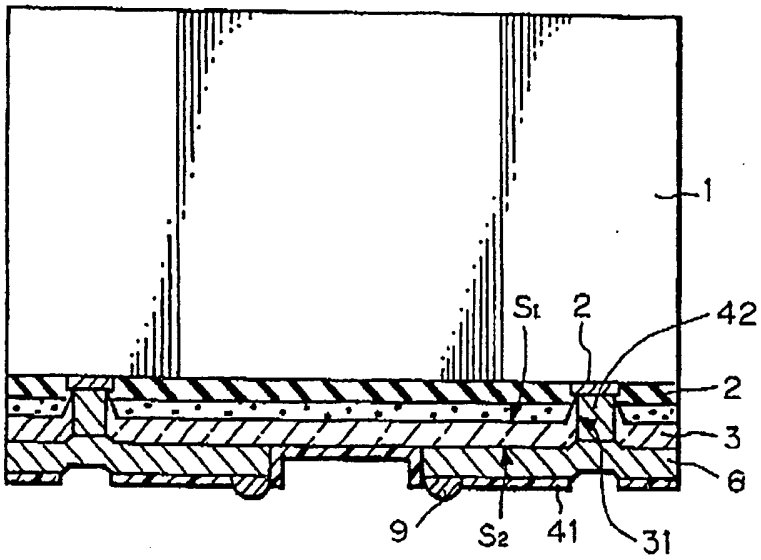


Fig. 13B

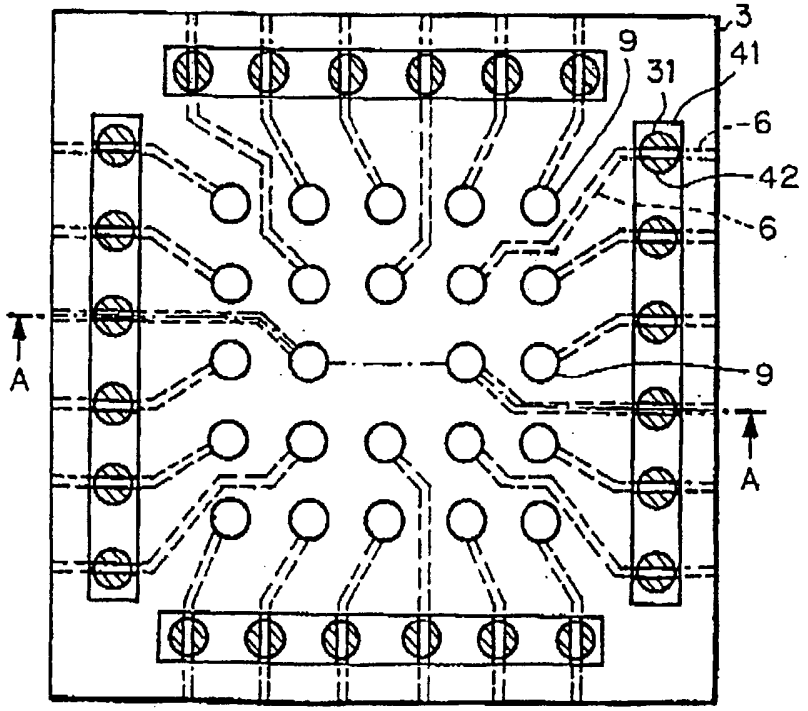


Fig. 14A

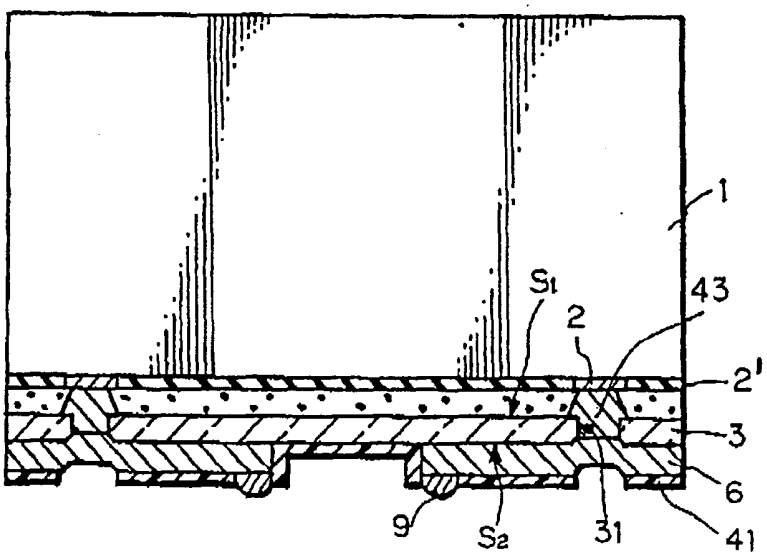


Fig. 14B

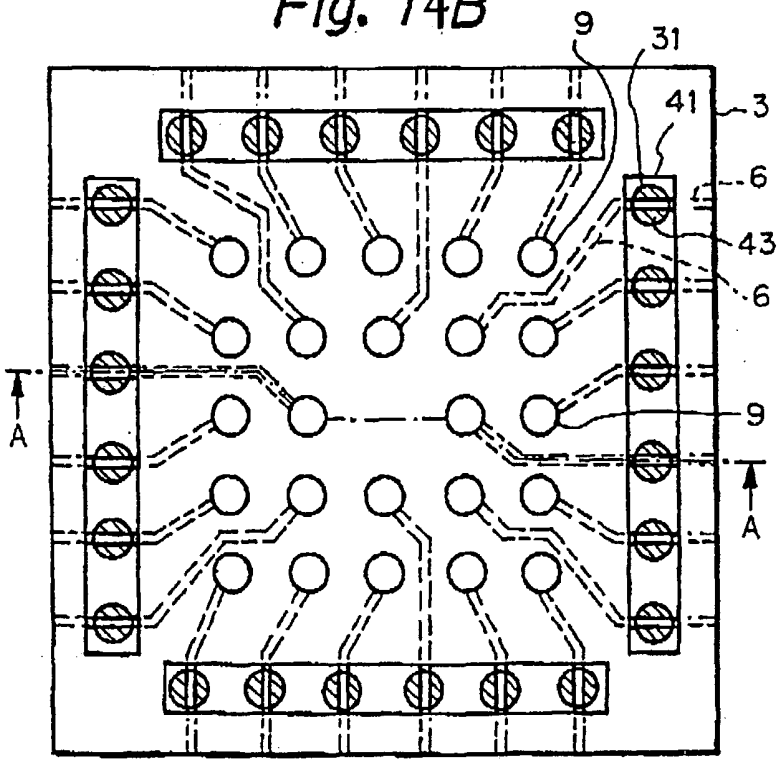


Fig. 15A

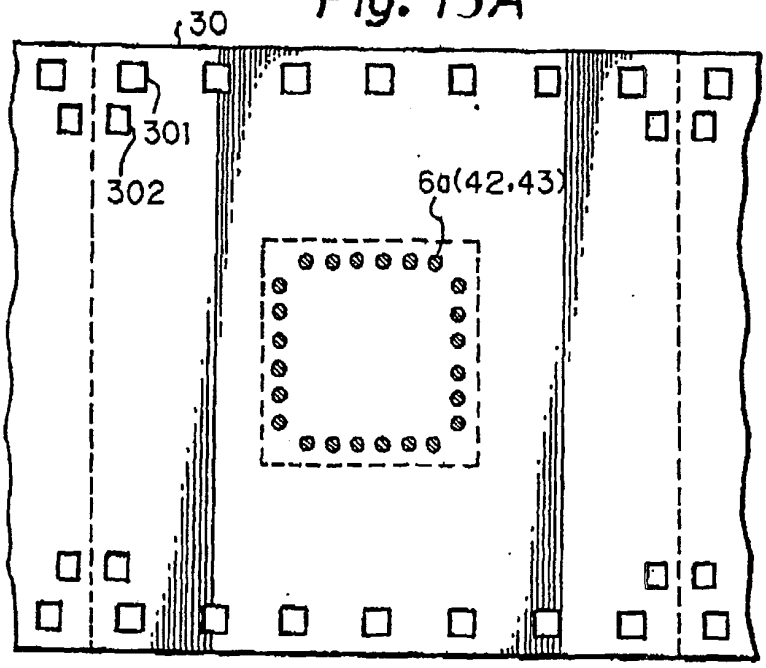


Fig. 15B

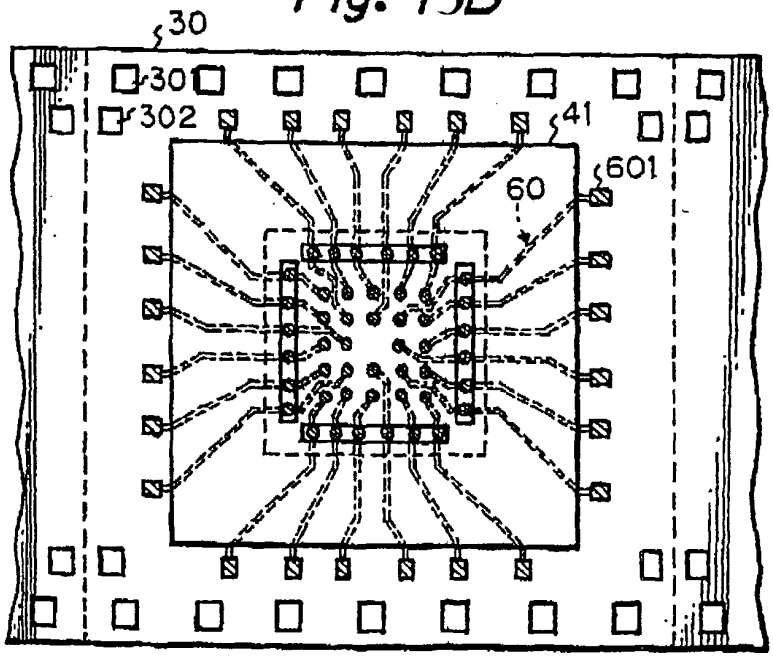


Fig. 16A

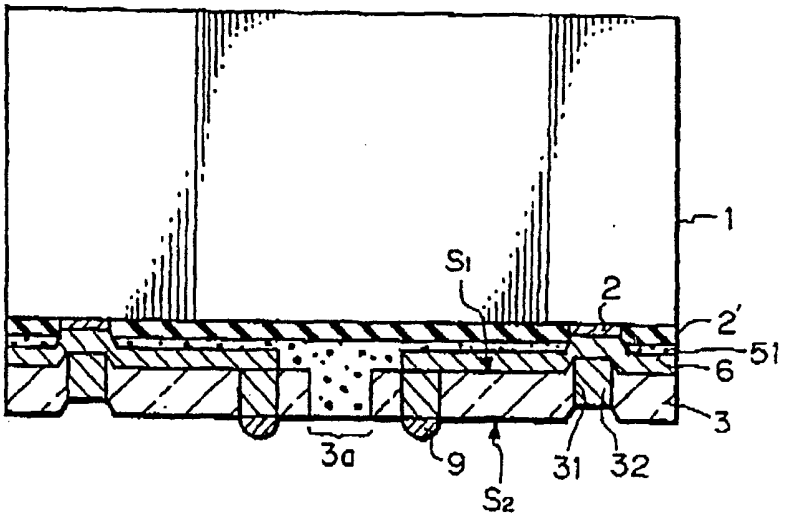


Fig. 16B

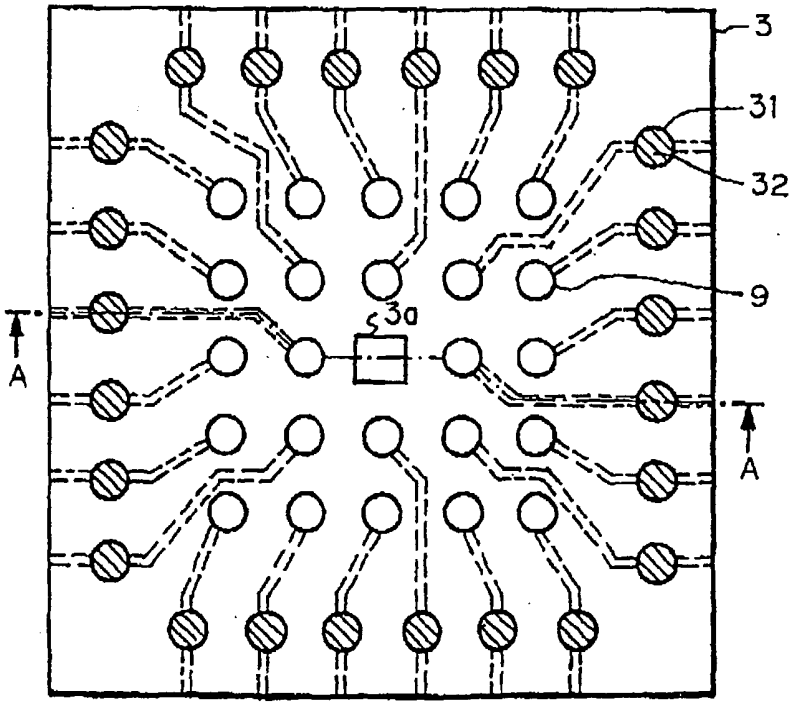


Fig. 17A

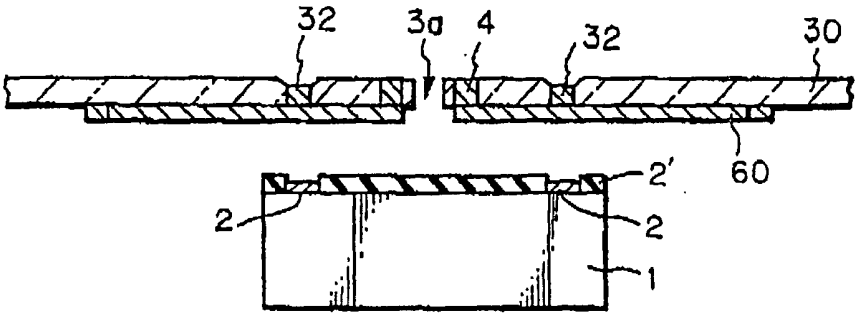


Fig. 17B

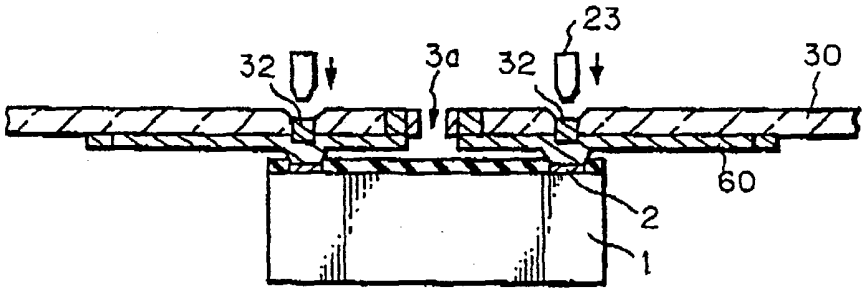


Fig. 17C

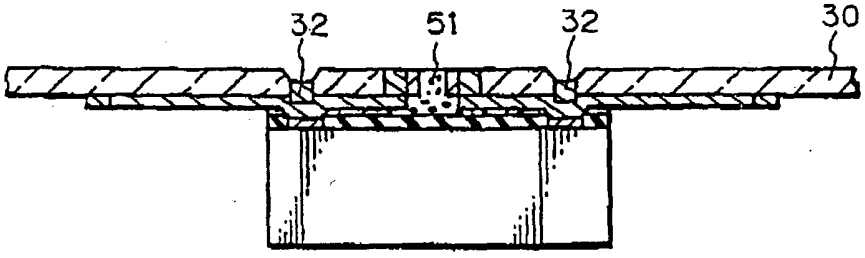


Fig. 17D

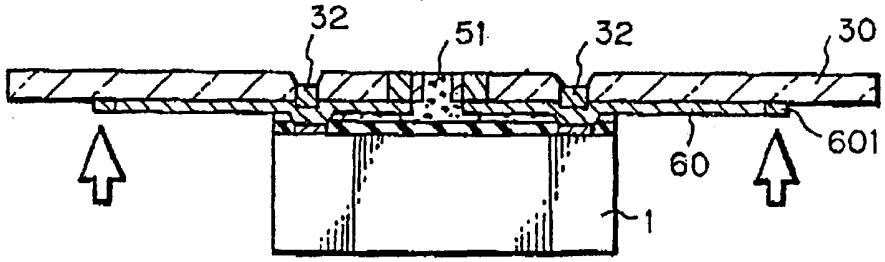


Fig. 17E

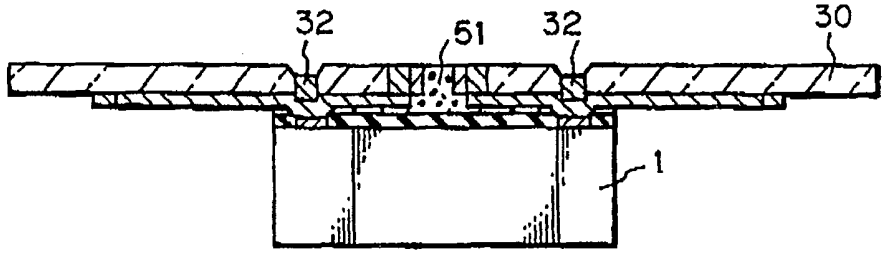


Fig. 17F

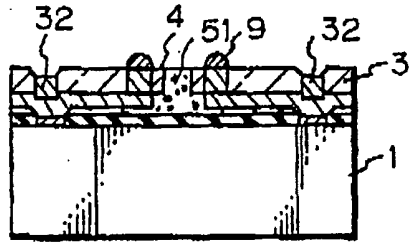


Fig. 17G

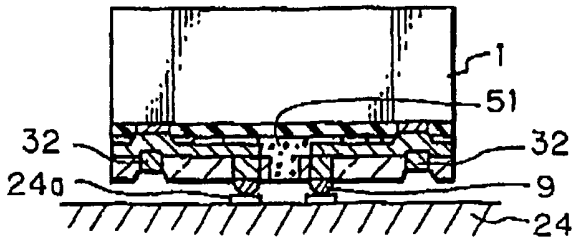


Fig. 18

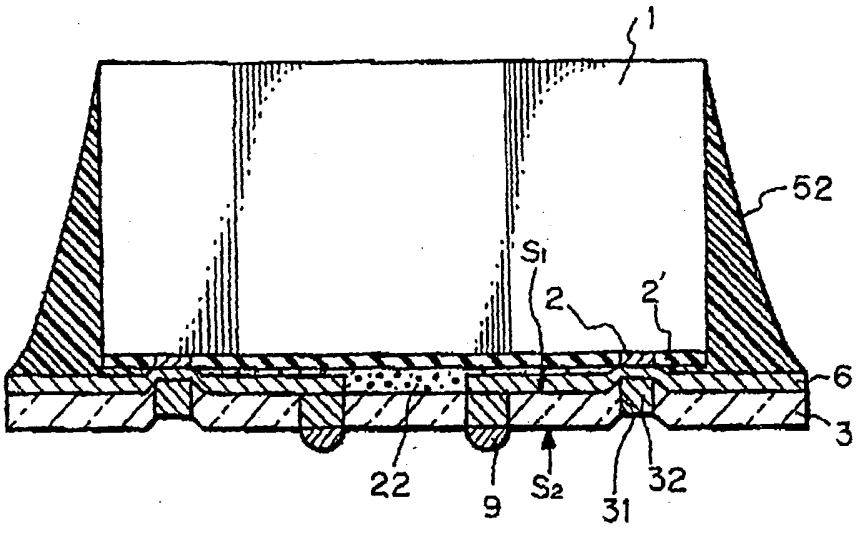


Fig. 19 A

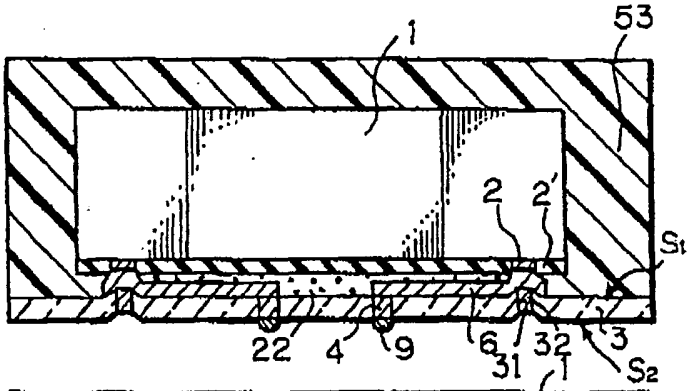


Fig. 19 B

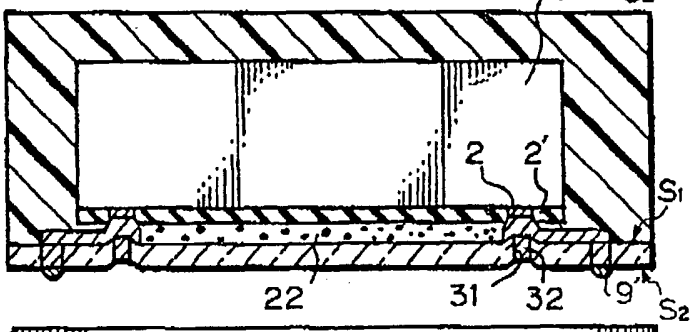


Fig. 19 C